Improving Bounds for FPGA Logic Minimization

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Abstract— **We present a methodology for improving the bounds of combinational designs implemented on networks of lookup tables, moving them closer to the theoretical minimum. Our work effectively extends optimality to span logic minimization and technology mapping. We obtain a proof of optimality by restricting ourselves to 4-input look-up tables (LUTs) and generating all possible circuits up to a certain area or latency depending on the optimization mode. Since simple-minded generation would take a long time, we develop levels of abstraction (steps) and techniques to restrict and order the search space, and produce results in practical time. We use logic decomposition to break up large designs, using the resulting trees to guide our search and prune the search space. The price of this optimality is that we are limited to small blocks; however, such blocks can be used to build larger designs.**

I. Introduction

We address the problem of identifying minimal circuits for a function by improving the upper and lower bounds of resources it can use. We find the lower bound using global generation: in principle, generating every possible configuration of a device. In pratice, we use local symmetries to give the effect of exhaustive generation at reduced cost, using Field-Programmable Gate Array devices (FPGAs) for high-speed emulation of configurations and connections of look-up tables (LUTs). By searching the space of LUT configurations and interconnections directly, we combine logic minimisation and technology mapping from Boolean functions to LUTs. We find the upper bound using logic decomposition, applying local generation on the components of the decomposition. If we are lucky, global generation uncovers the minimum possible implementation. Otherwise, we get an improved measure of the bounds within which the optimal design must lie, as well as a locally optimized implementation.

Our main contributions in this paper are to:

- Improve the measure of the bounds for optimal solutions
- Build a framework for circuit generation combining logic minimization and technology mapping
- Use logic decomposition to guide search, pruning the search space and giving the upper bound
- Evaluate our techniques on standard benchmarks

The rest of this paper is structured as follows: Section II gives an overview of our approach, comparing it with related work. Section III shows our circuit generation framework combining logic minimization and technology mapping. Section IV shows parallel hardware for generating circuits on FPGAs. Section V uses logic decomposition to guide and speed up the search, finding the upper bound. Section VI gives results and evaluates the use of logic decomposition in our framework for logic minimization and technology mapping. Finally, Section VII concludes and suggests future work.

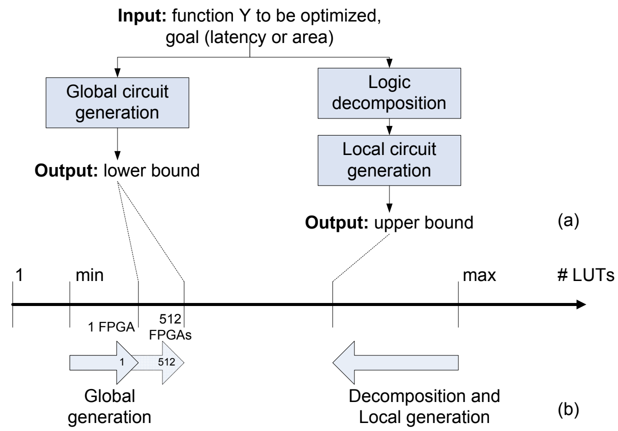

Fig. 1. Improving bounds by generation and decomposition: (a) Process input (logic function) and outputs (upper and lower bounds). (b) Starting with the initial maximum max and minimum min number of LUTs, global circuit generation increases the lower bound, while decomposition and local generation reduce the upper. Generation is parallelizable, so multiple FPGAs can be used for generation, allowing a higher lower bound by generating more circuits in a reasonable time. Ultimately we find either the absolute minimum circuit by global generation, or new, tighter bounds within which it must lie.

II. Overview and related work

Our approach improves the initial lower and upper bounds of the number of LUTs required to implement a given logic function. (fig. 1), using circuit generation and logic decomposition: global circuit generation, on the entire design, improves the minimum; local generation, on the parts of the decomposed design, improves the maximum.

We break generation into four steps (fig. 2). We implement step 4 in parallel hardware on FPGAs, relying on two key FPGA properties: (a) LUTs: high-speed table look-up. (b) Massive parallelism: many instances in parallel. We limit ourselves to single output functions; generation for multiple output functions is impractical.

Early works on area minimization decompose the circuit into a set of trees, and apply technology mapping on tree structures [1], [2]. Cong et al. concentrate on enumeration of single output, K-input connected subgraphs (fanout-free cones) within the circuit, and prove that the problem can still be optimally solved by decomposing the circuit into maximal fanout-free cones (MFFC), and enumerating separately on each MFFC [3]. The proposed algorithm restricts the solution

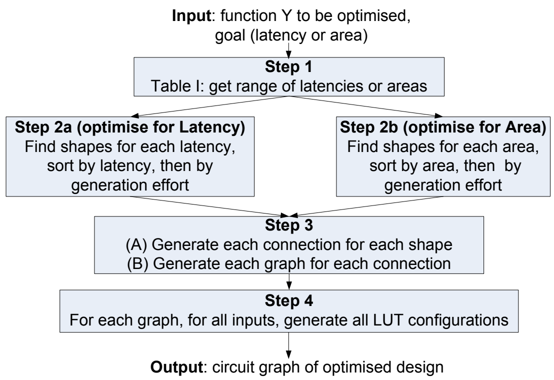

Fig. 2. Circuit generation. Step 2 differs for area (step 2a) and latency (step 2b). Step 4 can run in software or parallel hardware (section IV).

to duplication-free mappings where each circuit gate must be mapped to exactly one LUT. Later work by Cong et al. [4] introduces heuristics to reduce the runtime, and extends the approach to duplicable mappings.

More recently, Ling et al [5] reformulated the technology mapping problem as a Boolean satisfiability (SAT) problem, showing that state-of-the-art FPGA technology mapping algorithms miss optimal solutions. They also created an algorithm solving the optimal area mapping problem. Safarpour et al. [8] decompose the resulting SAT problem into two easier problems to increase efficiency. Cong et al. [9] derive their SAT formulation from the implicant rather than the minterm representation of the problem, creating a smaller problem which can be solved faster and cover more target problems.

Two recent efforts using enumeration concern an implicit technique for enumerating structural choices in circuit optimization based on rewiring and resubstitution [6], and the adoption of reverse search in enumerative optimization for obtaining, for instance, the k shortest Euclidean spanning trees [7]. Our research complements this work, since we exploit circuit parallelism to speed up generation.

III. Framework

This section shows our circuit generation framework's four-step approach, developing expressions for the upper and lower bound sizes of mappings from function to graph of LUTs. Fig. 2 shows how we break the problem into four steps: **Step 1**: given an N-bit input, 1-bit output boolean input function Y and an optimization mode (area or latency), identify observable inputs and limit the search space. **Step 2**: generate all circuit *shapes* (vectors of the numbers of LUTs in each layer) within the search space from step 1; sort by (a) latency or (b) area. **Step 3**: generate all possible interconnections for each shape, **Step 4**: generate all possible LUT configurations for each circuit graph. We generate graphs of 4-input LUTs, with H layers of LUTs, where layer h has L_h LUTs; L_{tot} LUTs in total.

Logic functions with more than four inputs require multiple LUTs. We further refine the steps of fig. 2 for N-input logic functions.

TABLE I

Step 1: Theoretical upper and lower bounds for latency (maximal depth of LUTs from inputs to output) and area (number of LUTs) for various numbers of inputs.

function	optimize for latency		optimize for area	
#inputs	min	max	min	max
≤ 4	1	1	1	1
5	2	2	2	3
N	$log_4(N)$	$(N-3)$	$\lfloor (N+1)/3 \rfloor$	$2^{N-3}-1$
	$O(logN)$	$O(N)$	$O(N)$	$O(2^N)$

Step 1 Count observable inputs, index into table I to find the area or latency bounds. We define *latency* as the maximal depth in LUTs from design inputs to design output, and *area* as the total number of LUTs. We calculate the initial upper bound by observing that an $n+1$-input design can be implemented using two n-input LUTs multipexed by an additional LUT controlled by the $n+1$th input.

Three rules facilitate calculation of minumum area and latency required: (1) each observable design input must connect to at least one LUT input, (2) at least one of the LUT inputs must connect to a LUT output at a previous layer, (3) there is a single LUT at the highest layer.

These rules ensure that (1) no input is redundant, (2) no LUT is disconnected (redundant) and (3) there is only one design output.

Step 2 Find all shapes for the bounds from step 1 (table II). Sort the resulting list of shapes by latency (if optimizing for latency, step 2a) or area (if optimizing for area, step 2b). Within the sorted list, sort equal-area (step 2a) or equal-latency (step 2b) shapes by generation effort: order by size of search space in steps 3 and 4. For example, for an 7-input design for minimum area, first choose the smallest shape that will accept seven inputs: (1,1) in our terminology. If this fails, choose the next smallest shape: (2,1). Similarly, find the minimum latency design by iterating from the minimum latency topology to the maximum. We observe that the number of shapes for a given number of LUTs L_{tot} and layers H is bounded by the binomial coefficient $\binom{L_{tot}}{H}$. Thus the total number of shapes is bounded by $2^{L_{tot}}$ [10], and the total number of shapes for the bounds of areas from step 1 is bounded by: $\sum_{\lfloor (N+1)/3 \rfloor}^{2^{N-3}-1} 2^{L_{tot}} = 2^{2^{N-3}} - 2^{\lfloor (N+1)/3 \rfloor}$

Step 3 Generate all interconnections. Step 3(A): produce a set of *connections* for each shape: topologically distinct trees where the output of each LUT in a layer must connect to the input of a LUT in the next layer. Step 3(B): generate directed acyclic *graphs* for each connection: all combinations of connections from each LUT input unconnected in step 3(A) to each LUT output in previous layers, and the design inputs. For a LUT at layer h, the number of possible interconnections is: $L_{h-1} * (N + \sum_0^{h-1} L_i)^3$.

Step 4 For all graphs, generate each configuration of each LUT, for each input. The output of the final circuit must match Y for each input over the input space of 2^N. We use parallel hardware to speed this step, shown in the next section.

TABLE II

STEP 2: ALL THE DIFFERENT SHAPES FOR ONE TO THREE 4-LUTS

		Latency			
		1	2	3	4
Area	1	(1)			
	2		(1,1)		
	3		(2,1)	(1,1,1)	

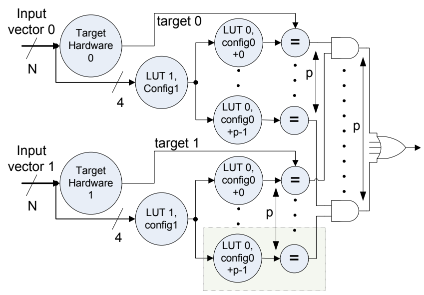

Fig. 3. (a) Hardware for parallel generation of shape (1,1), with $I = 2$ input vectors in parallel. For each input vector, we replicate the target hardware and emulation of LUT 1, and LUT 0 for each of p different configurations. We use this design for both breadth- and depth-first generation. Dotted lines indicate hardware omitted for clarity.

IV. GENERATION CIRCUIT GENERATION

This section shows our designs for implementing step 4 of figure 2 (generating all LUT configurations for each graph, for all inputs) by parallel generation on reconfigurable hardware.

We build FPGA circuits using ASC, A Stream Compiler [11]. For our implementation, this means we can write low-level optimizations and high-level structure all within the same C++ description. We build one ASC design per shape:

Step 4 Generate an ASC circuit for each graph output from step 3(B). Instantiate the target hardware, datapath containing LUT emulators and comparators, and a finite state machine to loop through each input until the first failing one, for each configuration, stopping at the first configuration that matches the target Y output for each input. We emulate LUTs, rather than use FPGA LUTs directly, to avoid reconfiguring the design for each set of LUT configurations.

Fig. 3 shows the datapath our parallel generation hardware, which we use for both depth-first and breadth-first approaches. The difference is in the state machine driving the datapath: depth-first tries each input until the first failing one; breadth-first tries only a small set of inputs. In this design, *failing* means that none of the configurations of LUT0 match the the target (output of Y) for all the parallel inputs.

Mapping to Xilinx LUTs. Part of the above design can map explicitly to Xilinx Virtex II CLB resources – similar techniques can apply to other FPGA families. Our hardware design has two properties: (a) for p LUTs emulated in parallel, each parallel configuration for LUT 0 lies in the same arithmetic sequence $c..c + p$, (b) thus the $log_2(p)$ least-significant bits of each configuration are constant, and can be emulated with ROMs.

V. LOGIC DECOMPOSITION

This section shows how we use logic decomposition to improve the measure of the upper bound number of LUTs needed to implement the target design from the initial maximum.

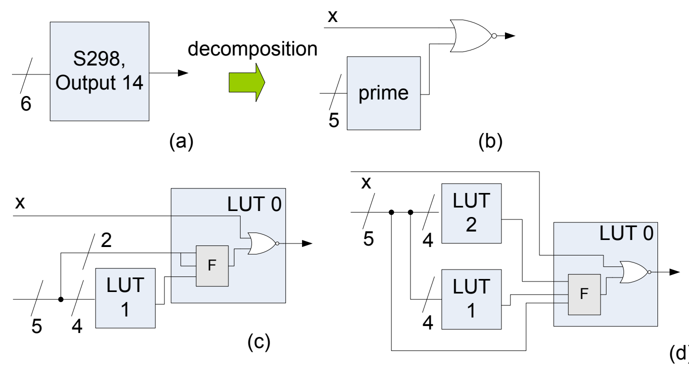

Fig. 4. Using logic decomposition: motivating example. One benchmark (a) is decomposed into a five-input function and a NOR gate with input labelled x (b). We show that only designs (c) and (d) need be considered, a considerably smaller search space than for a general six-input function, and for LUT 0, we need only generate three-input function F.

Logic decomposition takes a circuit and returns a collection of subcircuits and their connections, which, when composed together, give the same output as the input circuit.

To show the potential benefits of logic decomposition, consider a small example: output 14 of ISCAS benchmark s298. This has six observable inputs: too large to generate on a single CPU or FPGA. The total search space for a six-input function is of order $O(2^{128})$, using up to seven LUTs. Figure 4 shows the results of decomposing this design (a) into (b): a two-input NOR gate and a five-input prime (non-decomposable) block. After decomposition, we can reduce the search space to (c) and (d) : a five-input function takes at most three LUTs (d), and this design can implement the NOR in LUT 0. Three LUTs is a significant search-space reduction compared to seven without decomposition. Furthermore, because part of the function of LUT 0 is now fixed, its search space reduces to a three-input function F (d) (search space size $2^{2^3} = 2^8$, compared to 2^{16} for a 4-input function). The total search-space reduction is thus $2^{16}/2^8 = 256$. Also, the bounds improve from 2..3 (latency) and 2..7 (area) to 2..2 (latency) and 2..3 (area). Logic decomposition improves the upper bound, generating each subsearch separately. Although the overall result is no longer optimal, each generated subcircuit remains optimal.

Because circuit generation takes time exponential in the number of design inputs, we choose a disjoint decomposition method, so the decomposed functions have no common inputs; specifically, we use Plaza and Bertacco's STACCATO method and software [12]. Staccato decomposes a logic function into a tree of subfunctions, each with disjoint inputs. Each subfunction is either associative (AND, OR, XOR), or a *prime* function – one that cannot be decomposed further.

Our approach divides into four steps: (1) apply logic decomposition to design, (2) traverse the decomposition tree, separating out the prime (non-decomposable) blocks, (3) generate each prime block, (4) build the output hardware from the generated blocks. Step 3 applies the generation techniques

TABLE III

RANGE IMPROVEMENT. SHOWS NUMBER OF OBSERVABLE INPUTS, MINIMAL SHAPE FOUND AND RESULTS FROM XILINX XSTV8.1 AND FOR DAOMAP AND FLOWMAP, USING THE RASP PACKAGE FROM UCLA [13].

Name	Output	#Obs. Inputs	#Shapes	Shape	#LUTs XST	DAOmap	FlowMap	Area bounds (old)	(imp.)	Latency bounds (old)	(imp.)
s27	1	5	2	(1,1)	2	5	5	2..3	2..2	2..2	2..2
	2	5	2	(1,1)	2	2	2	2..3	2..2	2..2	2..2
	3	5	2	(1,1)	2	5	5	2..3	2..2	2..2	2..2
s298	8	5	2	(1,1)	2	3	3	2..3	2..2	2..2	2..2
	10	5	2	(1,1)	2	3	3	2..3	2..2	2..2	2..2
	12	7	268	(2,1)	3	5	5	2..15	3..3	2..2	3..3
	14	6	18	(2,1)	3	3	3	2..7	3..3	2..2	3..3
b01	4	5	2	(1,1)	2	3	3	2..3	2..2	2..2	2..2
	5	5	2	(1,1)	2	3	3	2..3	2..2	2..2	2..2
	6	5	2	(1,1)	2	3	3	2..3	2..2	2..2	2..2
	7	5	2	(1,1)	2	2	3	2..3	2..2	2..2	2..2

designed in the rest of this paper, using the global optimization goal (latency or area). Note that the decomposed prime blocks may still have too many inputs to practically generate; these cases must rely on conventional tools for optimization.

VI. RESULTS AND EVALUATION

This section shows results for software and hardware generation for several ISCAS benchmarks, showing original and improved bounds achieved.

Table III shows benchmarks chosen from the standard ISCAS 85, 89 and 99 sets, with bounds of LUTs for area and latencies – these worst-case results are the initial upper and lower bounds from table I. The XST, DAOmap [15] and FlowMap [14] results are for each output individually – we remove hardware for other outputs. The bounds improvement results for these benchmarks show runtime and minimal shapes found (software results run on an Intel Xeon 2Ghz processor).

Generation times vary up to an order of magnitude. All the software generation results correspond to an generation rate of roughly 4.8×10^6 configurations per second, about 20% the rate of our hardware. Hardware generation runs on a single Xilinx XC2V6000 FPGA (Celoxica RC2000 board).

VII. CONCLUSION

We show a methodology for optimising circuits for FPGA implementation that combines logic minimization and technology mapping. We develop a four-step process to give the effect of generating all possible circuits ordered by user optimization goal: latency or area. Our reconfigurable hardware implementation speeds this process by rapidly finding which generated circuits match the target design. We use logic decomposition to guide and speed our search process, eliminating searches using the resulting decomposition tree. Although our approach is only globally optimal for small designs, it is still locally optimal for larger designs, and can be applied to building blocks of larger designs.

Current and future work includes porting generation to a large multiple-FPGA machine. This is ideal for generation as many generators can run in parallel across multiple FPGAs. We would also like to extend generation to cover multiple-output designs, sequential designs and other design elements beyond LUTs. Our ultimate goal is to subsume many traditionally separate optimization steps into one generation step, with results guaranteed to be optimal.

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